

IN THE CLAIMS:

Cancel claim 5.

Please amend the claims as follows:

1. (Currently Amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each semiconductor substrate element of said substrate elements including integrated circuitry, comprising:
providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side in a first wafer having a periphery having a portion thereof including a flat;
providing a second semiconductor substrate element having a first side including integrated circuitry thereon and having a backside in a second wafer having a periphery having a portion thereof including a flat;
stacking said first semiconductor substrate element and ~~said the~~ [at least one] second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the second semiconductor substrate element having the periphery of said first semiconductor substrate element substantially aligned with the periphery of said second semiconductor substrate element, said first semiconductor substrate element and the second semiconductor substrate element for locating a portion of the integrated circuitry on said first semiconductor substrate element vertically spaced from [adjacent] a portion of the integrated circuitry on the second semiconductor substrate element for vertical alignment of said first semiconductor element and said second semiconductor substrate element; and severing from said stack transversely at least one dice pair comprising a die from said first semiconductor substrate element and a second die from said [at least one] second semiconductor substrate element; and

adhesively attaching said first semiconductor substrate element and said [at least one] second semiconductor substrate element.

2. (Original) The method of claim 1, wherein said adhesive comprises a dielectric adhesive.

3. (Amended) The method of claim 1, further including:
disposing a heat sink element between said first semiconductor substrate element and said [at least one] second semiconductor substrate element.

4. (Previously Twice Amended) The method of claim 1, wherein said first semiconductor substrate element and the second semiconductor substrate element, each semiconductor substrate element of the first semiconductor element and the second semiconductor element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. Canceled.

6. (Previously Amended) The method of claim 1, further comprising:
connecting a first die of said at least one dice pair to [conductors of] a substrate having conductors.

7. (Original) The method of claim 6, wherein said connection is selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. (Amended) The method of claim 6, further comprising:
connecting both dice of said at least one dice pair to said conductors of said substrate.

9. (Original) The method of claim 6, further comprising:
connecting the second die of said at least one dice pair to portions of the conductors of said
substrate through intermediate connection elements.
10. (Previously Amended) The method of claim 9, wherein said intermediate
connection elements are selected from a group consisting of bond wires and traces of flex
circuits.
11. (Previously Twice Amended) The method of claim 10, further comprising:
connecting said at least one dice pair to portions of the conductors of said substrate and
encapsulating said at least one dice pair thereafter.

REMARKS

Claims 1 through 4 and 6 through 24 are currently pending in the application.

Claim 5 has been canceled.

Claims 12 through 24 are withdrawn from consideration as being directed to a non-elected invention.

Claims 1 through 11 were rejected.

This amendment is in response to the Final Office Action of April 23, 2003 and the Advisory Action of July 1, 2003.

Applicant submits with this amendment a Request for Approval of Drawing Corrections for drawing FIG. 7 and a corrected Formal Drawing for drawing FIG. 7.. Applicant requests approval of such drawing corrections shown in red ink for drawing FIG. 7 and the entry of the corrected Formal Drawing for drawing FIG. 7.

Claims 1 through 11 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.


Applicant has amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Applicant has amended the claimed invention as set forth in claim 1 to include alignment of the first semiconductor substrate element and second semiconductor substrate element to clearly set forth the alignment of the elements as part of the claimed invention. Applicant submits that such amendment to claim 1 clearly sets forth the Applicants invention without omitting any necessary element of the claimed invention. Additionally, Applicant has amended the claimed invention to clearly provide antecedent for various terms as requested in the Office Action to particularly point out and distinctly claim the subject matter which Applicant regards as the invention to comply with 35 U.S.C. § 112, second paragraph. Therefore, presently amended claims 1 through 4 and 6 through 11 are allowable under the provisions of 35 U.S.C. § 112.

Additionally, Applicant has canceled claim 5 to comply with the comments in the Advisory Action of July 1, 2003.

Serial No. 09/943,880

In summary, Applicant requests the allowance of claims 1 through 4 and 6 through 11 and the case passed for issue.

Respectfully submitted,



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Date: July 17, 2003
JRD/sls:djp
Document in ProLaw